UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,524	08/07/2001	Chun Wang	ATI.0001670	1770

34456 7590 07/25/2005

TOLER & LARSON & ABEL L.L.P.
5000 PLAZA ON THE LAKE STE 265
AUSTIN, TX 78746

EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,524	WANG ET AL.	
	Examiner	Art Unit	
	Hau H. Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claims 1-34 is withdrawn in view of the newly discovered reference to MacInnis et al. (U.S. Patent No. 6,570,579). Rejections based on the newly cited reference follow.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim1-6, 8, 10-21, 23-32, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by MacInnis et al. (U.S. Patent No. 6,570,579).

Referring to claims 1, 19, and 21, as shown in Fig. 32, MacInnis et al. teach a dual memory controller system services memory requests generated by a display engine 1118, a CPU 1120, a graphics accelerator 1124 and an input/output module 1126 are provided to a memory select block 1100. The memory select block 1100 (a router) preferably routes the memory requests to a first arbiter 1102 or to a second arbiter 1106 based on the address of the requested memory. The first arbiter 1102 sends memory requests to a first memory controller 1104 while the second arbiter 1106 sends memory requests to a second memory controller 1108 (col. 53, lines 28-39). MacInnis et al. further teach each memory controller can support different configuration of SDRAM device types and banks, or other forms of memory besides SDRAM. The first and the second memory controllers may be accessed concurrently by different clients.

For example, a graphics memory may be allocated through the first memory controller while a CPU memory is allocated through the second memory controller. While a display engine is accessing the first memory controller, a CPU may access the second memory controller at the same time (col. 53, lines 1-27). Thus, besides the address of the requested memory as cited above, configuration data is inherently included to identify which memory controller will support the requesting client (either the CPU, the display engine, or the display controller).

In regard to claims 2-4, as shown in Figs. 1 and 2, MacInnis et al. teach the plurality of clients and memory controllers integrated in graphics chip 10, which also includes a graphics controller 64.

As for claim 6 with reference to FIG. 3, MacInnis et al. teach the graphics display system further includes an I/O bus 74 connected between the CPU 22, memory 28 and one or more of a wide variety of peripheral devices, such as flash memory, ROM, MPEG decoders, cable modems or other devices (col. 7, lines 33-38). Thus, it is implied that the plurality of clients include at least two clients having a common client type (e.g. two MPEG decoders).

In regard to claims 5, 8 and 10-14, as cited above, MacInnis et al. teach the first and the second memory controllers may be accessed concurrently by different clients, in which one client access the first memory controller, and another client access the second memory controller at the same time, and that two clients may be simultaneously pending at the first memory controller (please see the example on col. 53, lines 1-27). As shown in Fig. 33, McInnis et al. teach prioritizing access requests in a round robin arbitration scheme (col. 56, lines 20-53).

In regard to claims 15-16, MacInnis et al. teach the priority of the memory access requests is scheduled in real time (dynamic), and different arbitration scheme is performed

during processing based on the number of memory clock cycles of the memory access request (col. 55, lines 16-35).

As for claims 17-18, MacInnis et al. teach the priority assigned depends on a device identifier, and on an internal timer (a block out timer) (col. 56, lines 42-53).

In regard to claims 20 and 23, MacInnis et al. teach the number of the access requests routed to a memory controller from a particular client is dependent on a data rate of the particular client, and that the memory controllers can handle requests of varying data rates (col. 56, lines 20-31).

Referring to claims 24-26, as cited above with reference again to Fig. 32, MacInnis et al. teach a memory storage module, which inherently includes memory locations to store data, and an output port; a plurality of clients 1118-1126, each of which having a data access port; a router 1100 having a plurality of input ports coupled to the data access port of each of the plurality of clients; the router 1100 is to route data at each one of the input ports to a respective output ports to the memory based on the address of the memory access requests as cited above; a first memory controller is coupled to the first output ports of the router 1100, a second memory controller is coupled to the second output ports of the router 1100; and a first arbiter 1102 and second arbiter 1106 to select data access request on one of the first input ports to provide to the output port of the arbiters (col. 53, lines 28-39). As also cited above, MacInnis et al. teach at least two clients of the plurality of clients having common type.

In regard to claim 27, which is similar in scope to claim 13; therefore are rejected under the same rationale.

In regard to claim 28, which is similar in scope to claim 15; therefore are rejected under the same rationale.

In regard to claim 29, which is similar in scope to claim 8; therefore are rejected under the same rationale.

In regard to claim 30, which is similar in scope to claim 19; therefore are rejected under the same rationale.

In regard to claim 31, which is similar in scope to claim 20; therefore are rejected under the same rationale.

In regard to claim 32, which is similar in scope to claim 21; therefore are rejected under the same rationale.

In regard to claim 34, which is similar in scope to claim 20; therefore are rejected under the same rationale.

4. Claims 35-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Artieri (U.S. Patent No. 6,104,751).

Referring to claims 35, 36, 39, and 40, as shown in Fig. 3, Artieri teaches an MPEG decoder comprising a memory bus MBUS, couples the picture memory 15 to the compressed data input bus CDin, to the input of the variable length decoder (VLD) 10, to the input of the half-pixel filter 14, and to the input of a display controller 18. Exchanges on the memory bus MBUS are controlled by a memory controller (MCU) 24 that serves to carry out, upon request of the FIFOs, transfer operations between these FIFOs and the picture memory. To achieve this purpose, the memory controller 24 receives a plurality of requests RQ and provides corresponding acknowledgements ACK (col. 6, lines 34-51). As shown in Fig. 8, Artieri teaches

four MPEG decoders connected so as to process the four slices of the high definition picture. The input of each MPEG decoder is connected to the compressed data bus CDin, and each decoder operates with a respective picture memory (col. 20, lines 14-25). Also, between each decoder, there is provided an exchange system allowing a decoder to provide the data of its slice to its memory and to provide the same data to the memories of the adjacent decoders through an exchange bus XBUS (col. 20, lines 59-67, and col. 21, lines 1-14).

In regard to claim 37, Artieri teaches the memory controller to read the blocks in the first buffer memory and to write them in the picture memory at addresses corresponding to the specific slice, and to read the blocks in the second buffer memory and to write them at addresses corresponding to a margin (Fig. 9, col. 5, lines 53-65).

In regard to claims 38 and 41, Artieri teaches the system includes a plurality of processing elements using decoding parameters, and a memory bus controlled by a memory controller to exchange data between the processing elements at rates adapted to the processing rates of these elements, and to store in a picture memory data to be processed or re-used (col. 3, lines 40-49).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis et al. (U.S. Patent No. 6,570,579) in view of Kilgariff et al. (U.S. Patent No. 5,999,183).

Referring to claims 7 and 9, as cited above, MacInnis et al. teach that at least two clients are of common type, and that one client is accessing a first memory controller while the other client is accessing a second memory controller at the same time. Thus, MacInnis et al. teach all the limitations of claims 7 and 9, except that the common client type includes one of two-dimensional graphics driver, three-dimensional graphics driver, or an audio driver; and the first memory controller executes a first portion of an access request, the second memory controller executes a second portion of the access request.

However, Kilgariff et al. teach a scalable, three-dimensional (3D) graphics subsystem as shown in Fig. 5, comprising a plurality of graphics modules 500_1 –500_4 coupled together through one or more routing devices. These graphics modules 500_1-500_4 may include the first graphics module 500_1 (shown as module 210 of FIGS. 2-4) and the second graphics module 500_2 (shown as module 410 of FIG. 4); a routing device 510 establishes a communication link (e.g., an electrical connection) between four (4) memory controllers of rendering modules 520_1-520_4 of graphics modules 500_1–500_4, respectively (clients of common type are graphics drivers). Each memory controller of each rendering module 520_1 . . . , 520_4 is coupled to routing device 510 through its expansion port (col. 5, lines 4-24). Each rendering module processes a pixel region (executes a portion of an access request).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by MacInnis et al. in combination with the method as taught by Kilgariff et al. in order to provide a graphics subsystem that offers scalable performance with efficient use of memory (col. 2, lines 11-13).

7. Claims 22 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis et al. (U.S. Patent No. 6,570,579) in view of Foster et al. (U.S. Patent No. 6,240,492).

Referring to claims 22 and 33, as applied to claims 1 and 24 above, MacInnis et al. teach all the limitations of claims 22 and 33, except for each memory controller receives an HDTVstream.

However, Foster et al. teach an integrated system architecture 10' for a high definition digital video decoder is depicted in FIG. 2. In this architecture, an integrated circuit chip 12' includes multiple functional units B & C, with generic functional unit A shown to comprise a High Definition Television (HDTV) video decoder 14'. The HDTV video decoder includes two memory ports, with port 1 being coupled to dedicated bus 22 for accessing dedicated memory 26 through dedicated memory controller 24, and port 2 coupled to the general system bus 16 for accessing shared memory 20 through common memory controller 18 (col. 6, lines 19-36).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Foster et al. in combination with the method as taught by MacInnis et al. in order to minimize costs of the overall architecture and enhance performance (col. 6, lines 40-42).

Response to Arguments

8. Applicant's arguments filed April 27, 2005 with respect to claims 35-41, have been fully considered but they are not persuasive. In response to Applicant's arguments that reference Artieri does not teach receiving a client request from a video decoder, routing the client request to a memory controller, the examiner disagrees. As cited in the previous Office Action, with reference to Fig. 3, Artieri teaches exchanges on the memory bus MBUS are controlled by a

memory controller (MCU) 24 that serves to carry out, upon request of the FIFOs, transfer operations between these FIFOs and the picture memory. To achieve this purpose, the memory controller 24 receives a plurality of requests RQ and provides corresponding acknowledgements ACK (col. 6, lines 34-51). Thus, the routing of client request is handled by the MBUS to the memory controller 24, and the client request is received for the video decoder, which comprises elements 10-14, 16, 18, 21, 22, and 26, as shown in Fig. 3. With reference further to Fig. 8, as also cited in the previous Office Action, Artieri teaches four MPEG decoders connected so as to process the four slices of the high definition picture. Thus, as cited above, each memory controller receives a client request from a corresponding video decoder.

Since reference Artieri meets the minimum requirement of claim 35, rejection is maintained.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778.

The fax number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-2 17-9197 (toll-free).

H. Nguyen

07/13/2005

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600